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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/366,768	08/04/1999	JONATHAN WADE AIN	TU999033	3462

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EXAMINER

PHAN, TRI H

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/366,768

Applicant(s)

AIN ET AL.

Examiner

Tri H. Phan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 June 2002 and 12 January 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-48 is/are pending in the application.
- 4a) Of the above claim(s) 1-10 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20,30 and 39 is/are allowed.
- 6) ☒ Claim(s) 11-14,21-24,31-33 and 40-48 is/are rejected.
- 7) ☒ Claim(s) 15-19,25-29 and 34-38 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 20, 30 and 39 is objected to because of the following informalities:

- In Claim 20, Line 19, the recitation "locating the 32-bit word comprising said destination address," is ended with a period in the middle; therefore, the claim (Claim 20) is unclear where it is completed.

- Claim 30, Line 16, and Claim 39, Line 16 are rejected for the same objection's reason given in Claim 20.

Applicant is required to provide appropriate corrections.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim 14, Lines 6-7, it recites the limitation "said encoder". There are insufficient antecedent bases for this limitation in the claim 14, neither in the parent claims (Claim 11 and 13).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 11-14, 21-24, 31-33 and 40-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Berman** (U.S.6,118,776) in view of **Beckner et al.** (U.S.4,833,671).

- In regard to claims 11, 21 and 31, **Berman** discloses *a method to limit access to information using a fibre channel arbitrated loop system* (For example see Col. 4, Lines 20-26) *comprises the steps of inspecting and determining the source addresses and the destination addresses included in the incoming data frame* (For example see Col. 10, Lines 64-66; wherein the source and destination addresses are disclosed in Col. 9, Lines 12-16), *providing permitted address information* (For example see Col. 11, Lines 40-45; Col. 14, Line 64 through Col. 15, Line 2). **Berman** does disclose about the 'match/no match' bit in the receiving frame as disclosed in Col. 14, Line 64 through Col. 15, Line 2, but fails to disclose about "idle character". However, such implementation is known in the art.

For example, **Beckner** discloses that *inspecting and determining the source addresses and the destination addresses included in the incoming data frame* (For example see Col. 9, Lines 50-66; Col. 10, Lines 31-45; for checking a proper header of the incoming data frame),

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providing an IDLE character generator (idle frame), determining if the incoming data frame is addressed to an unconfigured source address/destination address pair (For example see Col. 9, Lines 45-65; determining if the incoming data frame is pack with the header, wherein the source and destination addresses include in the header is just an inherence), operative if the incoming data frame is not addressed to an unconfigured source address/destination address pair, allowing the data frame to pass to the destination address (For example see Col. 9, Line50-66; wherein if the header is ready or correct, then operative) and operative if the incoming data frame is addressed to an unconfigured source/destination addressed pair, replacing the incoming data frame with IDLE characters (For example see Col. 10, Lines 5-20; Col. 11, Lines 30-40; wherein if the incoming data frame is not ready or incorrect, generating an empty frame for transmission).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of “*providing an IDLE character generator, allowing the data frame to pass to the destination address if the incoming data frame is not addressed to an unconfigured source address/destination address pair, or replacing the incoming data frame with IDLE characters if the incoming data frame is addressed to an unconfigured source/destination addressed pair*” as taught by **Beckner** in **Berman**’s system with the motivation being to improve the ability to detect and restrict access information in the network.

- Regarding claims 12 and 22, **Berman** further discloses *wherein the incoming data frame comprises a request to access information, further comprising the step of disallowing*

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access by the incoming data frame to the requested information (For example see Col. 11, Lines 40-54; Col. 14, Line 60 through Col. 15, Line 24).

- In regard to claims 13, 23 and 32, **Berman** further fails to disclose *the method comprises the steps of receiving serial data comprising the data frame, converting the serial data to parallel data, wherein the parallel data comprises the source address and the destination address, comparing the parallel data to the permitted address information, operative if the incoming data frame is not addressed to an unconfigured source/destination addressed pair, converting the parallel data to the serial data.* However, such implementation is known in the art.

For example, **Beckner** discloses that *receiving serial data comprising the data frame (sdi) and converting the serial data to parallel data (pdi), comparing the parallel data to the permitted address information (permitted header), operative if the incoming data frame is not addressed to an unconfigured source/destination addressed pair and converting the parallel data to the serial data (sdo) (For example see Figs. 4-5; Col. 15, Lines 10-55; operative if the incoming data frame is not proper header).*

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of *"receiving serial data comprising the data frame, converting the serial data to parallel data, wherein the parallel data comprises the source address and the destination address, comparing the parallel data to the permitted address information, operative if the incoming data frame is not addressed to an unconfigured source/destination addressed pair, converting the parallel data to the serial data"* as taught by

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Beckner in **Berman**'s system with the motivation being to improve the method to detect and restrict access information in the network.

- Regarding claims 14, 24 and 33, **Berman** further fails to disclose *the method comprises the steps of placing the parallel data into a regulator, providing a trigger circuit, wherein the trigger circuit is in communication with the regulator, operative if the incoming data frame is not addressed to an unconfigured source/destination addressed pair, triggering the regulator to pass the parallel data to the encoder.* However, such implementation is known in the art.

For example, **Beckner** discloses that *placing the parallel data into a regulator, providing a trigger circuit, wherein the trigger circuit is in communication with the regulator* (For example see Col. 9, Lines 58-62), *operative if the incoming data frame is not addressed to an unconfigured source/destination addressed pair, triggering the regulator to pass the parallel data to the encoder* (For example see Fig. 5).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of "*placing the parallel data into a regulator, providing a trigger circuit, wherein the trigger circuit is in communication with the regulator, operative if the incoming data frame is not addressed to an unconfigured source/destination addressed pair, triggering the regulator to pass the parallel data to the encoder*" as taught by **Beckner** in **Berman**'s system with the motivation being to improve the method to detect and restrict access information in the network.

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- In regard to claims 40, 43 and 46, **Berman** discloses *the blocking apparatus to limit access to information in a fibre channel arbitrated loop system* (For example see Col. 4, Lines 20-26) *comprises a decoder (decoder module), wherein the decoder is capable of communication with one or more communication networks* (For example see Fig. 17; Col. 14, Lines 15-22, 62-64), *permitted address information (address table; For example see Col. 13, Lines 4-25), a comparator (address match module), wherein the comparator is capable of communication with the decoder and with the permitted address information* (For example see Col. 13, Lines 26-50; Col. 14, Line 64 through Col. 15, Line 2), *an encoder (encoder module; For example see Fig. 17; Col. 14, Lines 15-22, 62-64)*, but fails to disclose *an IDLE character generator, wherein the IDLE character generator is capable of communication with the comparator, a trigger circuit, wherein the trigger circuit is capable of communication with the comparator, a regulator, wherein the regulator is capable of communication with the decoder and with the trigger circuit and an encoder, wherein the encoder is in communication with the regulator*. However, such implementation is known in the art.

For example, **Beckner** discloses that *the blocking apparatus to limit access to information in a fibre channel arbitrated loop system* (For example see Col. 16, Lines 15-20; wherein the system could be used in a fibre channel arbitrated loop system) *comprises a decoder, permitted address information, a comparator (controller 68 and 70 in Fig. 6), an IDLE character generator (an empty frame generator) is capable of communication with the comparator, a trigger circuit* (For example see Col. 9, Lines 59-66) *is capable of communication with the comparator, a regulator is capable of communication with the decoder and with the trigger circuit* (For example see Fig. 6; Col. 14, Lines 15-60).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of "*an IDLE character generator is capable of communication with the comparator, a trigger circuit is capable of communication with the comparator, a regulator is capable of communication with the decoder and with the trigger circuit*" as taught by **Beckner** in **Berman**'s system with the motivation being to improve the system ability to detect and restrict access information in the network.

- Regarding claims 41-42, 44-45 and 47-48, **Berman** further fails to disclose *the apparatus comprises a deserializer is capable of communication with the decoder, a data first in / first out block is capable of communication with the decoder and with the comparator, a multiplexor is capable of communication with the comparator, the IDLE character generator and the data first in / first out block, a serializer is capable of communication with the encode.* However, such implementation is known in the art.

For example, **Beckner** discloses *the apparatus comprises a deserializer is capable of communication with the decoder, a data first in / first out block is capable of communication with the decoder and with the comparator, a serializer is capable of communication with the encoder, a multiplexor is capable of communication with the comparator, the IDLE character generator and the data first in / first out block* (For example see Figs. 5 and 6; Col. 5, Lines 55-67).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the implementation of "*the apparatus comprises a deserializer is capable of communication with the decoder, a data first in / first out block is*

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capable of communication with the decoder and with the comparator, a multiplexor is capable of communication with the comparator, the IDLE character generator and the data first in / first out block, a serializer is capable of communication with the encoder” as taught by Beckner in Berman’s system with the motivation being to improve the system ability to detect and restrict access information in the network.

Allowable Subject Matter

6. Claims 15-19, 25-29 and 34-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 20, 30 and 39 are allowed. The following is an examiner's statement of reasons for allowance:

Claims 20, 30 and 39 are considered allowable since when reading the claims in light of the specification, none of the references of record-alone or in combination disclose or suggest the combination of limitations specified in the independent claims including.

Substantially regarding claim 20, the prior art of record fails to disclose all the method steps using to limit access to information in the fibre channel arbitrated loop system which comprise receiving an incoming data frame comprising serial data, providing a deserializer, providing the serial data to the deserializer, converting the serial data to a plurality of ten bit

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parallel words, providing a regulator, providing the plurality of parallel words to the regulator, providing a trigger circuit being in communication with the regulator, providing a decoder, providing the plurality of parallel words to the decoder, packaging the plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte, providing a data first in/first out block, providing the 32-bit words to a data first in/first out block, detecting a start of frame signal, locating the 32-bit word comprising the source address and the destination address, providing permitted address information, providing an encoder, providing an IDLE character generator, comparing the source address to the permitted address information, operative if the source address does not match the permitted address information, replacing each of the 32-bit words with IDLE characters, operative if the source address matches the permitted address information, comparing the destination address to the permitted address information, operative if the destination address does not match the permitted address information, replacing each of the 32-bit words with IDLE characters, operative if the destination address matches the permitted address information by triggering the regulator to pass the parallel data to the encoder, converting the plurality of parallel words to the serial data and passing the serial data to the destination location.

Substantially regarding claims 30 and 39, the prior art of record fails to disclose all the program steps and program codes which support the method steps in claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

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fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Johnson et al. (U.S.6,888,800) and **Hagglund et al.** (U.S.6,584,101) are all cited to show devices and methods for improving switching in the telecommunication architectures, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan whose telephone number is (571)272-3074. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on (571)272-3126.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703)872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703)305-3900.



Tri H. Phan
May 27, 2005


BRIAN NGUYEN
PRIMARY EXAMINER